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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,147	09/24/2003	Kazi Asaduzzaman	A1068	7383

45851 7590 12/23/2005

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EXAMINER

TRAN, VINCENT HUY

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/670,147		ASADUZZAMAN ET AL.	
	Examiner		Art Unit	
	Vincent T. Tran		2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20-26 is/are allowed.
- 6) ☒ Claim(s) 1-6, 12 and 17 is/are rejected.
- 7) ☒ Claim(s) 7-11, 13-16, 18 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 9/24/03 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>9/24/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-26 are pending for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Goode U.S. Patent 4,953,185.

4. As per claim 1, Goode discloses a programmable logic device integrated circuit clock and data recovery circuit that recovers digital data and an embedded clock from an incoming serial data stream [col. 4 line 65 to col. 5 line 4], the clock and data recovery circuit comprising;

a first phase-locked loop [250 fig. 2] that locks onto a reference clock [290 fig. 2] when the clock and data recovery circuit is operated in a reference mode [Free-run mode – col. 6 lines 41-68];

a second phase-locked loop [230 fig. 2] that locks onto the incoming serial data stream [123 fig. 1] when the clock and data recovery circuit is operated in a data mode [Receive mode – col. 5 line 63 to col. 6 line 4]; and

a control circuit [260 fig. 2] that automatically switches the clock and data recovery circuit between the reference mode and the data mode [col. 7 lines 22-39].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2-3, 5, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goode as applied to claim 1 above, and further in view of Garlepp et al. U.S. Patent 6,920,622.

7. As per claim 2, Goode teaches a control circuit operable to automatically switch between the reference mode and the data mode. However, Goode does not teach the control circuitry is responsive to an override signal that forces the clock and data recovery circuit out of the automatic mode.

Garlepp et al. teach another clock circuit that includes a phase locked loop that generates an output clock wherein the output clock may be a multiple of a received reference clock. Garlepp et al. teach the selection of which input clock is utilized may be automatic selection or may be manual selection; wherein when in an automatic mode, the switching [control circuit 1550 fig. 15] of inputs may be automatically accomplished base upon predetermined condition in order to provide a stable clock to the system until an input clock is again valid [col. 17 lines 30-37; col. 18 lines 42-65]. Specifically, Garlepp et al. teach the control circuitry is responsive to an override signal [1553 fig. 15] to force the clock circuit out of the automatic mode and into a specific clock selected by the device [col. 17 lines 39-41, 58-61].

Goode and Garlepp et al. are analogous art because they from similar problem solving area; obtaining the stable clock for a system.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of with a control circuitry of Garlepp et al. that is responsive to an override signal to forces the circuit out to the automatic mode.

The motivation for doing so would have been to provide the system the ability to operate at a specific clock depended on the desire operation.

Therefore, it would have been obvious to combine Goode with Garlepp et al. to obtain the invention as specified in claim 2.

8. As per claim 3, see discussion in claim 3.

9. As per claim 5, Goode teaches a switch circuitry, wherein the control circuit automatically switches between the first PLL and the second PLL. However, Goode does not teach the control circuit includes circuitry responsive to the override signal and wherein when the override signal is asserted, the control circuitry directs the switch circuitry to switch the second PLL into use.

Garlepp et al. teach a control circuit [1550 fig. 15] includes circuitry responsive to a override signal [1553 fig. 15] to force the control circuitry to directs the switch circuitry to switch to a specific frequency.

Therefore, at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuitry of Goode with the override signal of

Garlepp et al. in order to provide the system the ability to operate at a specific clock depended on the desire operation.

10. As per claim 6, see discussion in claim 6.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goode as applied to claim 1 above, and further in view of Saito US 20020145480.

12. As per claim 4, Goode teaches a control circuit that automatically switches the clock circuit between the two mode of operation. However, Goode does not teach a charge pump having a switch circuitry.

Saito teaches another circuit which generates an oscillator signal that ensures the generation of stable internal control signal. Specifically, Saito teach a charge pump having switch circuitry, wherein the control circuit switches the switch circuitry to use the charge pump in generating the first frequency or the second frequency depended on whether the system is in the first or second operating state of the system [paragraph 0019].

At the time of the invention was made, it would having been obvious to of ordinary skill in the art to have modified the circuitry of Goode with the charge pump having switch circuitry of Saito to generate voltage control signal to the voltage controlled oscillator since the charge pump circuit is well know in the art.

13. Claims 12, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goode in view of Doblar et al. U.S. Patent 6,516,422.

14. As per claim 12, it is noted that the limitation do not substantially differ from claim 1, with the exception of the limitation reciting “the control circuit receives an override signal, the control circuit exits the automatic mode.” As demonstrated previously, the system of Goode anticipated the limitations in claim 1. However, Goode does not teach expressly, when the control circuit receives an override signal, the control circuit exits the automatic mode.

Doblar et al. teach another system and method for providing multiple synchronized clocks in a system, wherein the system includes a switching logic to monitor the first clock signal and the second clock signal. Doblar et al. teach the switching logic automatically switches the clock signal depended on the condition of the clock signal. Specifically, Doblar et al. teach switching logic upon receives an override signal would exits the automatic mode [col. 7 lines 5-11].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Goode with the override signal to force the control circuit to exit from the automatic mode as taught by Doblar et al. in order to provide the system the ability to operate at a specific clock depended on the desire operation.

15. As per claim 17, Goode teaches at least one detector [280, 270 fig. 2] that produces at least one signal indicative of whether the first phase-locked loop has locked onto the reference clock, wherein the control circuit uses the at least one signal in automatically moving the clock and data recovery circuit from reference mode to data mode [col. 7 lines 22-39; col. 8 lines 7-25].

Allowable Subject Matter

16. Claims 7-11, 13-16, 18, 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. Claims 20-26 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran



**CHUN CAO
PRIMARY EXAMINER**